

New Multi-Scale Simulation Framework for Next-Generation Electronic Design Automation with Application to the Junctionless Transistor

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In this paper we present a new multi-scale simulation scheme for next-generation electronic design automation for nano-electronics. The scheme features a combination of the first-principles quantum mechanical calculation, semi-classical semiconductor device simulation, compact model generation and circuit simulation. To demonstrate the feasibility of the proposed scheme, we apply our newly developed quantum mechanics/electromagnetics method to simulate the junctionless transistors. The simulation results are consistent with the experimental measurements and provide new insights on the depletion effect of the hetero-doped gate on the drain current. Based on the calculated I-V curves, a compact model is then constructed for the junctionless transistors. The validity of the compact model is further verified by the transient circuit simulation of an inverter.

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I. INTRODUCTION

The continuous miniaturization of semiconductor devices has resulted in the 22nm transistors and is expected to approach 10nm and beyond before 2026¹. Atomic features and quantum effects have become more pronounced than ever before, and some are even exploited as functioning mechanism of a range of new devices, such as transistors based on quantum dots² and wires³. The major challenges of the existing electronic design automation (EDA) tools are in how to incorporate the quantum phenomena into the classical semiconductor device models based on the continuum assumption. Full atomistic quantum mechanical (QM) calculation, while providing us with reliable characterizations of nano-scale systems, confronts severe applicability limitation due to the prohibitive computational cost. One natural solution is the multi-scale method, where only a small portion of the device is characterized with QM description and the remaining (non-critical) parts of the device plus the surrounding structures are treated classically. The rationale behind lies in that the QM effects that have substantial influence on device properties are confined to a small region, outside which (e.g., in the bulk material) classical models suffice to provide reasonable characterizations.

One element of this programme, namely a multi-scale quantum mechanics/electromagnetics (QM/EM) simulation framework that combines a first-principles QM simulator and a semi-classical EM solver, has already been delivered by the LODESTAR code^{4,5}, which achieves a high performance-cost-ratio that cannot be achieved otherwise. The QM/EM method has been applied to simulate the carbon nanotubes embedded in silicon substrates, and the good agreements with full QM simulation have been obtained.

Physics-based simulation of individual devices, such as the QM and QM/EM simulations mentioned above, comprises only one part in the modern EDA flow. One level upward the technology hierarchy, compact modeling of device is another necessity to enable computer simulation involving millions of devices in circuit simulation programme, such as SPICE⁶. State-of-the-art compact models of transistors, such as the BSIM family, are based on a process called parameter extraction, to determine a set of model parameters by fitting the measured I-V curves. The experimental data required to generate compact models are usually costly to obtain, in terms of both time and expense, particularly for emerging devices and structures for which experiments may not be available or mature enough to provide reliable data.

The objective of this paper is to report a multi-scale flow for next-generation EDA tools that spans from the first-principles QM simulation to the generation of the compact models for circuit simulations. To the knowledge of the authors, it is the first time that such a flow is reported in the literature. To demonstrate the feasibility of the entire flow, we apply the QM/EM method to the simulation of a new type of semiconductor device, the junctionless transistor, and generate a compact model based on the QM/EM results, which is then put into a circuit simulator to simulate a simple integrate circuit made of the junctionless transistors.

II. QM/EM SIMULATION

A. Basic Framework

The QM/EM method starts with partitioning the system of interest into QM regions which are described by quantum mechanics, and EM regions where classical models will be used. Typical domains that should be treated at QM level in a nanotransistor include the channel and parts of the source and drain for conduction currents. We did an external QM calculation with the gate included to demonstrate the quantum depletion effect caused by the hetero-doped gate. The EM regions consist the remaining parts of the system.

The QM part of the system is solved by using our first-principles simulator *LODESTAR*⁷, with the density-functional tight-binding (DFTB) method combined with the non-equilibrium Green's function (NEGF) method⁸. The EM solver combines the Maxwell's equations and the drift-diffusion (DD) model, as described in references^{9,10}. More advanced technology computer-aided design (TCAD) models for semiconductor devices can be readily used to replace the DD model for higher modeling requirements.

The two solvers are coupled via boundary conditions at the interfaces of the QM and EM regions. The EM solver is first applied in the whole domain to obtain an initial potential distribution. The potentials at the QM/EM interface then act as the boundary conditions for the QM calculation. In return, the current density through the QM/EM interface calculated by the QM solver is served as a part of the boundary conditions for the EM solver. The process is iterated until the current and potential at the interface converge. For more details we refer the readers to our previous papers^{4,5}.

B. Application on Junctionless Transistor

In this section, we apply the QM/EM method to simulate a new type of semiconductor device, junctionless transistor. The junctionless transistor revives in responding to the increasing difficulty in fabricating P-N junctions in devices smaller than 10nm, which requires an abrupt doping variation (e.g., from P-type to N-type) within a few nanometers and results in high electrical interference between source and drain. Basing on the ideas of Lilienfeld in the 1920s¹¹ and more recent calculations¹², Colinge *et al.* presented the first experimental realization of the junctionless transistor in 2010¹³. The channel of the device is made of an uniformly-doped silicon nanowire, and a hetero-doped gate, viz., the gate doped with different type of dopant from the channel, is used to deplete the carriers inside the channel and keeps the transistor “OFF” in the absence of an applied gate voltage. Positive or negative gate voltage is required to turn “ON” the device. Detailed measurements^{14–18}, as well as atomistic scale simulations^{19,20} were followed up by the same group. The success of the junctionless transistor has attracted great attention of both experimentalists and theorists^{21–25} in the world.

The structure of the junctionless transistor is shown in Fig. 1. The QM/EM region is divided differently in the ground state and steady state calculation. The QM region for ground state calculation includes a 6nm-long silicon nanowire doped by 6 Ga/As atoms along the (110) direction, which includes the source, channel and drain, and a “II” shaped hetero/homo-doped gate (the gate doped with the same/different type of dopants). From this calculation we obtain the free particles distribution in the absence of the applied gate voltage and the bias voltage, which gives us the figures of the depletion effect; When the QM/EM method is applied to the more time consuming steady state calculation, the QM region is further cutted down to a 3 nm long silicon nanowire, as shown in Fig. 1, the blue region. The EM region consists the remaining parts of the structure in the EM box with the size of $8 \times 6 \times 6 \text{ nm}^3$, which is very difficult to be handled as a whole by the exists atomistic QM simulators.

The depletion effect of a hetero-doped gate was characterized in the previous reports through an artificial work function difference between the transistor and the electrons to shift the “OFF” state to zero gate voltage both classically and quantum mechanically^{15,22}, where the value of the “shifting” is simply given as the difference of the Fermi levels of the

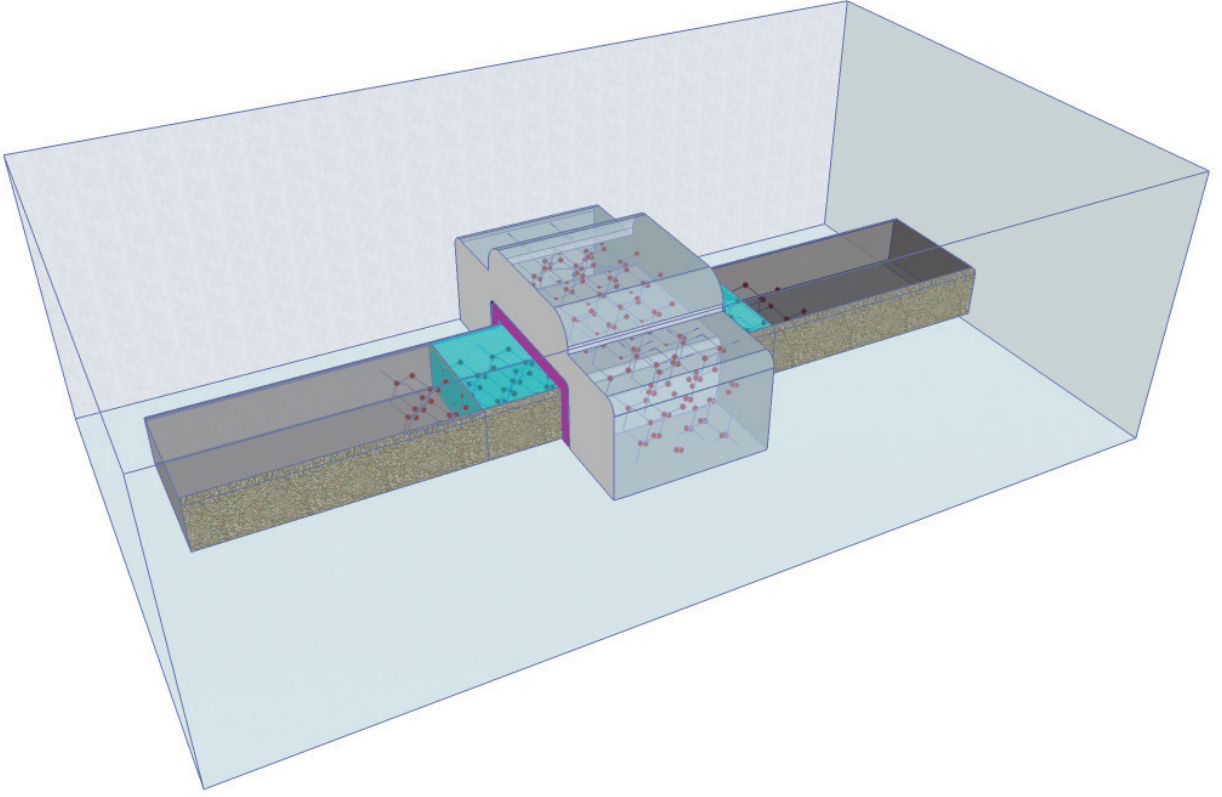


FIG. 1. The schematic representation of the QM/EM structure. QM/EM region is divided differently in the ground state and steady state calculation. A 6 nm long silicon nanowire with the cross section of $2.0 \times 1.5 \text{ nm}^2$ doped by 6 Ga/As atoms and the Π shaped gate above it are included in the ground state QM calculation; When the QM/EM method is applied to the steady state calculation, the QM region is further cutted down to a 3 nm nanowire (shown as blue region). EM part: The remaining part of the $8 \times 6 \times 6 \text{ nm}^3$ EM box.

N- and P-doped bulk silicon. In reality, the depletion effect is more complicated than the simple shifting of the Fermi level in the channel area. With explicit QM account of the gate, we are able to calculate the effect of the intrinsic work function difference more accurately.

In order to demonstrate the impact of the gate doping, we simulate four structures with the same geometry but different doping combinations, and plot in Fig. 2 the 6 electrons which occupy the highest occupied states in the N-channel devices (a,c) and the 6 holes which occupy the lowest unoccupied states (b,d). A temperature of 6K is introduced to help the convergence, resulting in a certain occupation above the Fermi level. The distribution of the free electrons in the N-channel device is obtained by $\rho_e(r) = \sum_{N/2-2}^N O_i \phi_i^*(r) S \phi_i(r)$, and

can be seen in Fig. 2 (a) and (c). And the distribution of the free holes in the P-channel device is obtained by $\rho_h = \sum_1^{N/2+2} (2.0 - O_i) \phi_i^* S \phi_i$ which has been seen in Fig. 2 (b) and (d). Here N is the number of electrons, S the overlap matrix, ϕ_i the eigenfunction and O_i the occupation.

Fig. 2 shows that, with homo-doped gate, no carrier depletion occurs, and the device is normally “ON” without gate bias. With hetero-doped gate, on the other hand, a significant portion of the carriers in the silicon nanowire is depleted to the gate, which results in the lack of carriers inside the channel and a great reduction in the conductivity of the transistor in the absence of the applied gate voltage. Positive or negative gate voltage is required to “push” the free carriers back to the channel and turn on the device. By controlling the doping type of the gate, one can construct either a depletion-mode transistor, which is “ON” at zero bias, or an enhancement-mode transistor, which is “OFF” at zero bias.

We also simulate the density of state (DOS) of the channel region. DOS in the absence of gate voltage and in a certain gate voltage has been obtained for the four different doped structures, as illustrated in Fig. 3 (a), (b), (c) and (d) corresponding to the structures (a), (b), (c) and (d) in Fig. 2. The atomic structures of the QM regions of (a) and (c) are identical while the calculated Fermi levels are different, resulted from the depletion effect of the hetero-doped gate which attracts the carriers to the gate (see Fig. 2 (c) and (d)). The difference near the Fermi level is clearly shown in Fig. 3 (a) and (c) when comparing the solid purple lines that represent the DOS in the zero gate bias. Similar analysis can be applied in Fig. 3 (b) and (d). The DOS figures show the electronic structures insights of the “ON/OFF” character of the transistors.

To generate the compact model for the junctionless transistor, we simulate the $I - V_{gate}$ curves for the hetero-doped and the homo-doped structures under the source-drain bias of 0.2V, and display them in Fig. 4. Since multiple simulations are needed to sample the gate voltages, and only the transport dynamics in the channel are of interest, we model the gate region with the EM simulator to reduce the burden of QM solver and speed up the computation. In the hetero-doped structure, the conducting current in channel is very low in the absence of a gate bias due to the lack of free carriers. When positive/negative gate voltage is applied, the carriers “absorbed” by the gate are driven back to the channel and switch the device from “OFF” to “ON”. On the contrary, the device with homo-doped gate is normally “ON” at zero gate voltage and is turned “OFF” when a gate voltage is applied

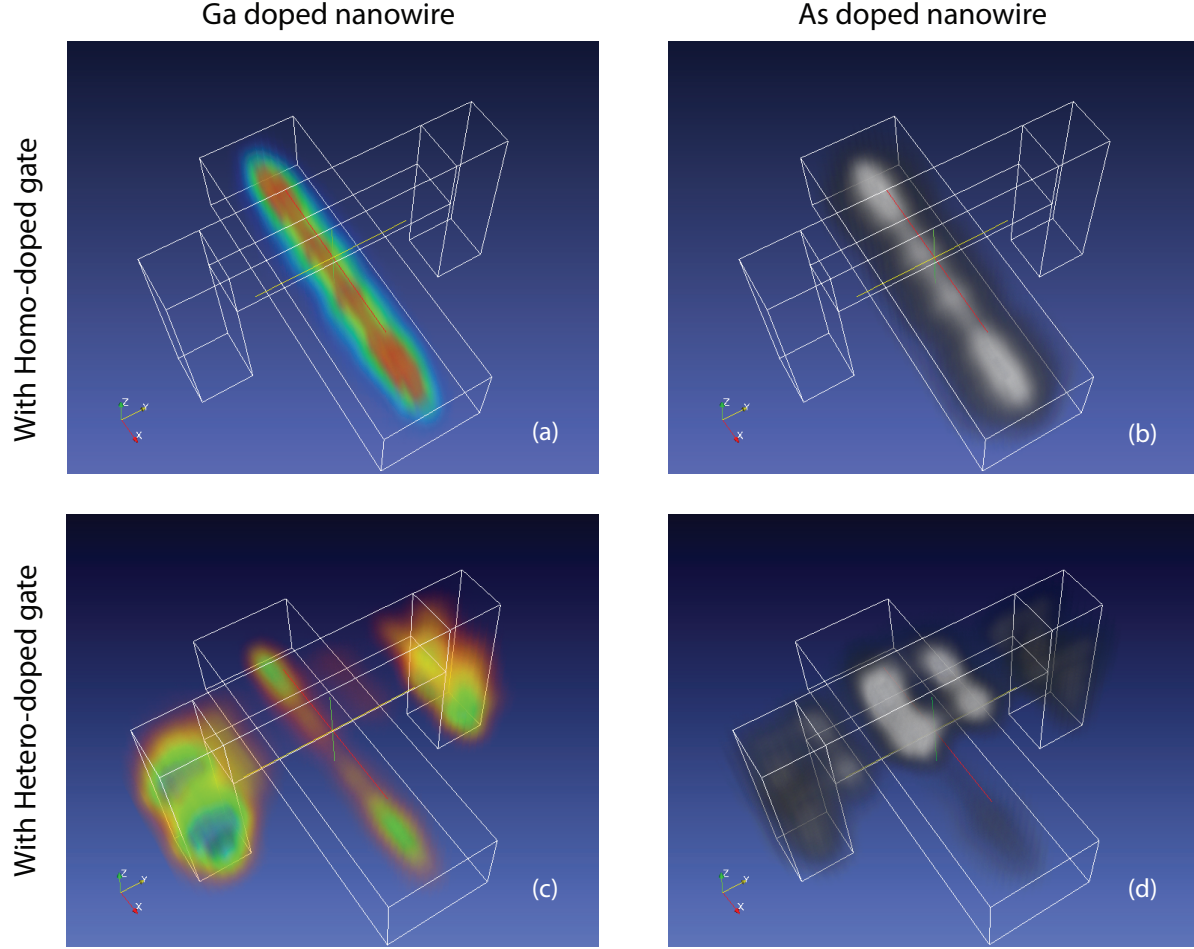


FIG. 2. Free electrons (6 in total) distribution in the N-channel nanowire with homo-doped gate (a) and with hetero-doped gate (c) ; free holes (6 in total) distribution in the P-channel nanowire with homo-doped gate (b) and with hetero-doped gate (d). In both (c) and (d), the free particles have been depleted by the hetero-doped gate.

to squeeze the carriers out of the channel.

Although the $I - V_{gate}$ curves are qualitatively consistent with the experimental results¹³, the magnitude of the “OFF” current is several orders larger than the curves in the measurements. The reason lies in the limited size of the QM region that can be handled by our first-principles simulator. Two dopants in a $3 \times 2 \times 1.5 \text{ nm}^3$ silicon wire leads to an equivalent doping concentration of $2.6 \times 10^{20} \text{ cm}^{-3}$, which is about one order higher than the ordinary values $2 \sim 5 \times 10^{19} \text{ cm}^{-3}$ for junctionless transistors. Such heavy doping density renders the silicon wire behave more like a conductor, and therefore, leads to relatively large

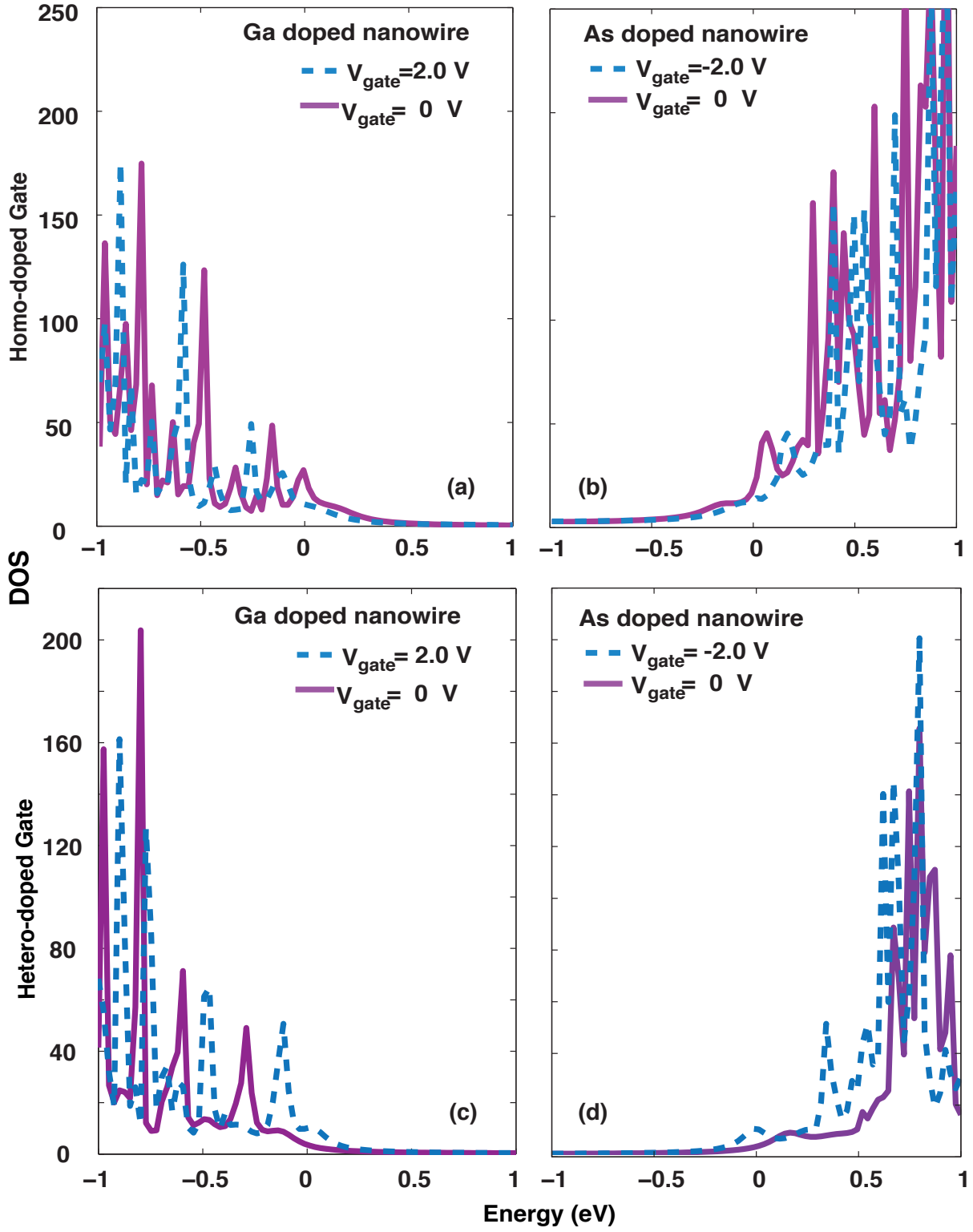


FIG. 3. Density of States (a),(b),(c),(d) correspond to structure (a),(b),(c) and (d) in Fig. 2. The purple solid lines represent the DOS without applied gate voltage, which are rich in figures (a) and (b) while, because of the hetero-doped gates, poor in figures (c) and (d) around the Fermi level. Positive or negative gate voltage is applied to shift the DOS to the blue dotted lines hence the ON/OFF states of the devices are changed.

current even at the “OFF” state. Meanwhile, the ultrashort gate length ~ 1 nm may cause the quantum barrier not large enough to prevent the electrons from tunneling through the channel, which can also result in the large “OFF” current.

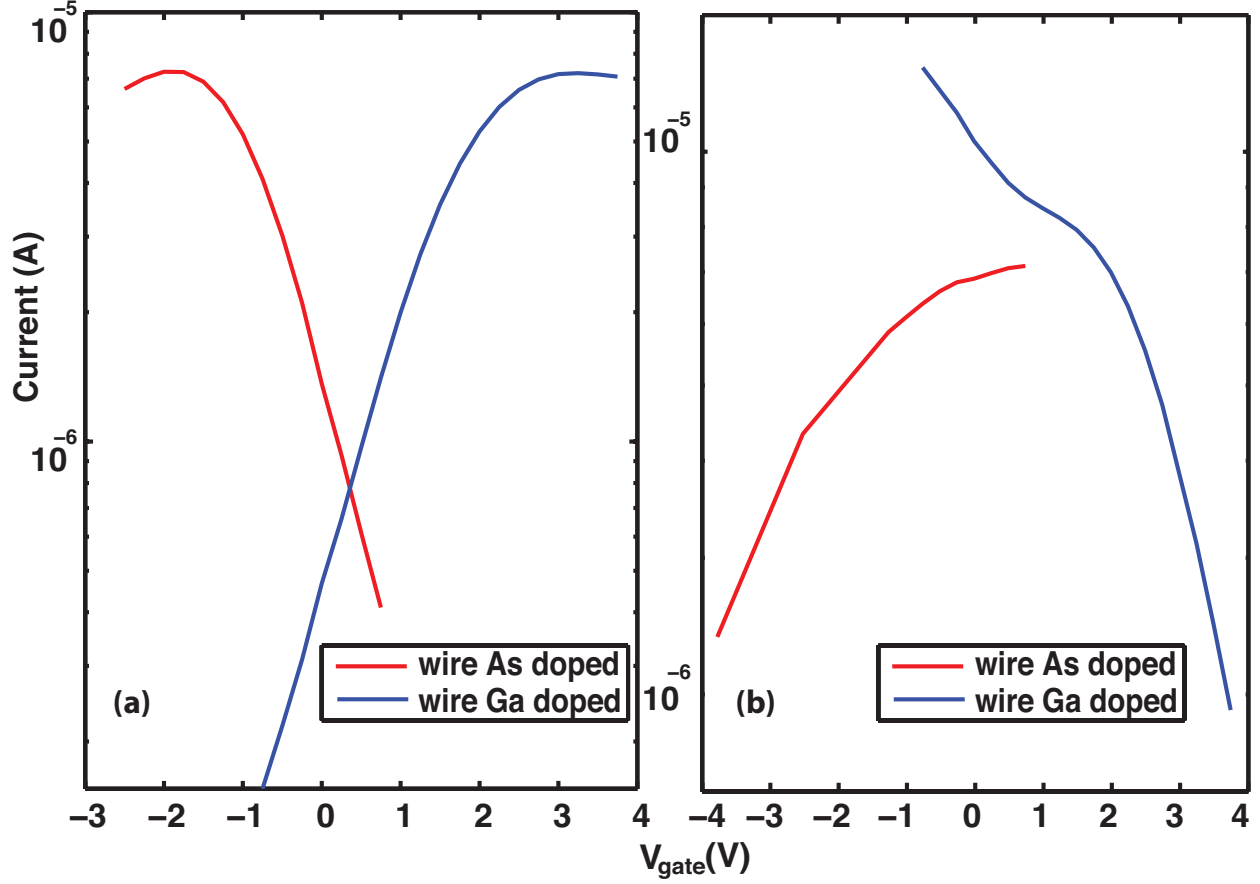


FIG. 4. $I - V_{gate}$ curves for hetero-doped structures (a) and homo-doped structures (b).

III. COMPACT MODELING

Parameter extraction is the essential part of compact modeling for semiconductor devices. The ultimate objective of our method is to replace the experimental data required in the parameter extraction process by the QM/EM simulation results. A direct connection between first-principles simulation and SPICE-compatible compact models helps to minimize costly experiment measurements and facilitate the modeling of emerging semiconductor devices from first-principles.

To demonstrate the multi-scale QM/EM-to-SPICE modeling process, we generate a prim-

itive compact model for junctionless transistor out of the I-V curves shown in Fig. 4 (a). Our compact model formulation is based upon a recently developed model²⁶ for the junctionless transistors. The operations of junctionless transistor are partitioned as linear, saturation and subthreshold regions according to the gate bias. The drain-to-source currents I_{ds} are modeled separately in the three regions. Several modifications are made to the original model²⁶ to render it suitable for our problem.

In the linear region, where the gate-to-source voltage V_{gate} is larger than the threshold voltage V_{th} and the drain-to-source voltage is small ($V_{gate} < V_{gate} - V_{th}$), the current through the device I_{ds} is linearly proportional to V_{gate}

$$I_{ds} \approx 2\mu \frac{\varepsilon_{ox}}{\beta t_{ox}} \frac{W}{L} \left(V_{gate} - V_{th} + \Delta V_{th} - \frac{V_{ds}}{2} \right) V_{ds} \quad (1)$$

where $\beta = 1 + \varepsilon_{ox} t_{si} / (4\varepsilon_{si} t_{ox})$ with ε_{si} and ε_{ox} being the permittivity of silicon and silicon oxide, and t_{si} and t_{ox} being the thickness of the silicon channel and the thickness of the silicon oxide layer between the gate and the channel, respectively. W and L are respectively the width and length of the device, and N_{si} is the doping concentration of the channel. The threshold voltage V_{th} is determined by

$$V_{th} = V_{fb} - \frac{qN_{si}t_{si}t_{ox}}{2\varepsilon_{ox}} - \frac{qN_{si}t_{si}^2}{8\varepsilon_{si}} \quad (2)$$

where V_{fb} is the flat band voltage of silicon. Since the structure in our simulation is ultra short and narrow, we introduce ΔV_{th} as a shift of the threshold voltage to take into account the short channel effect (SCE) and drain induced barrier lowering (DIBL)²⁷. The mobility μ is calculated by

$$\mu = s_{lin} \frac{L}{W} \frac{1}{V_{ds}} \frac{1}{C_i} \quad (3)$$

in which s_{lin} is the slope of I-V curve measured in the linear region and $C_i = 2\varepsilon_{ox} / (t_{ox}\beta)$ is the gate insulator capacitance per unit area.

When $V_{ds} \gg V_{gate} - V_{th} > 0$, the I-V curve enters the saturation region, where the drain current is expressed by

$$I_{ds} = \mu \frac{\varepsilon_{ox}}{\beta t_{ox}} \frac{W}{L} \left[(V_{gate} - V_{th} + \Delta V_{th})^2 - \frac{v_T \beta t_{ox}}{\varepsilon_{ox}} \sqrt{2qN_{si}\pi v_T \varepsilon_{si}} e^{(V_{gate} - V_{th} + \Delta V_{th} - V_{ds})/v_T} \right] \quad (4)$$

where v_T is the thermal voltage kT/q .

The subthreshold region (or the “OFF” region) occurs when $V_{gate} < V_{th}$. In this region, I_{ds} is described by

$$I_{ds} = \mu_{sub} v_T \frac{W}{L} \sqrt{2qN_{si}\pi v_T \varepsilon_{si}} e^{(V_{gate} - V_{th} + \Delta V_{th})/(v_T n_{slope})} (1 - e^{-V_{ds}/v_T}) \quad (5)$$

Here a different mobility is applied in the sub-threshold region $\mu_{sub} = \alpha\mu_{lin}$, wherein $\alpha > 1$ an adjustable coefficient. The amplified sub-threshold mobility is defined in such a way to accommodate the large subthreshold current observed in our simulation. The slope factor n_{slope} is used to modify the subthreshold slope for short-channel devices²⁷.

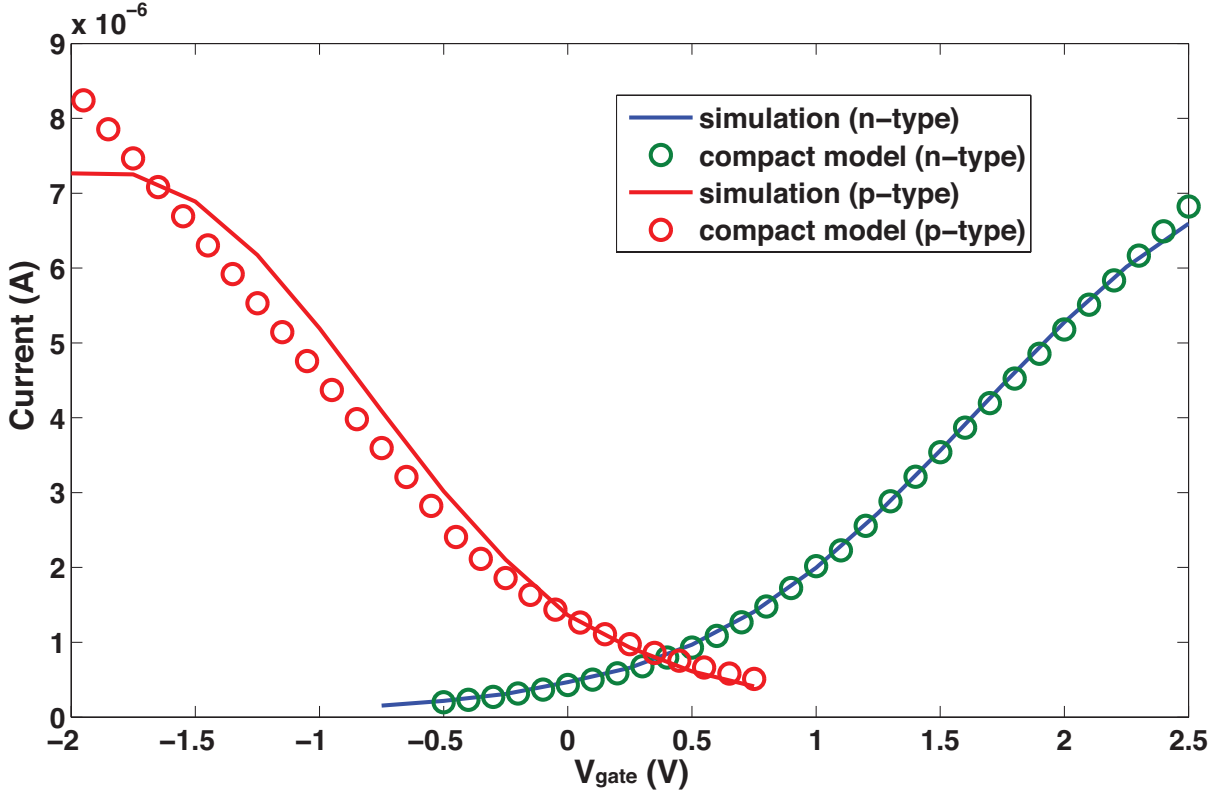


FIG. 5. $I - V_{gate}$ curves from QM/EM simulation and compact modeling.

The $I - V_{gate}$ curves in Fig. 4 (a) are fitted into the compact model by using equations (1), (4) and (5), as shown in Fig. 5. In addition, we incorporate the generated compact model into a Matlab-based SPICE-like simulator SMORES²⁸ to simulate an inverter circuit. The inverter, as shown in Fig. 6 (a), consists of an n-type and a p-type junctionless transistor. The transient circuit simulation result is shown in Fig. 6 (b). The output waveform is generally “inverted” from the input waveform, which verifies the functionality of the inverter. The peak-valley voltage difference in the output is relatively small, due to the low ON/OFF current ratio. It is expected that a higher ON/OFF ratio improves the voltage difference.

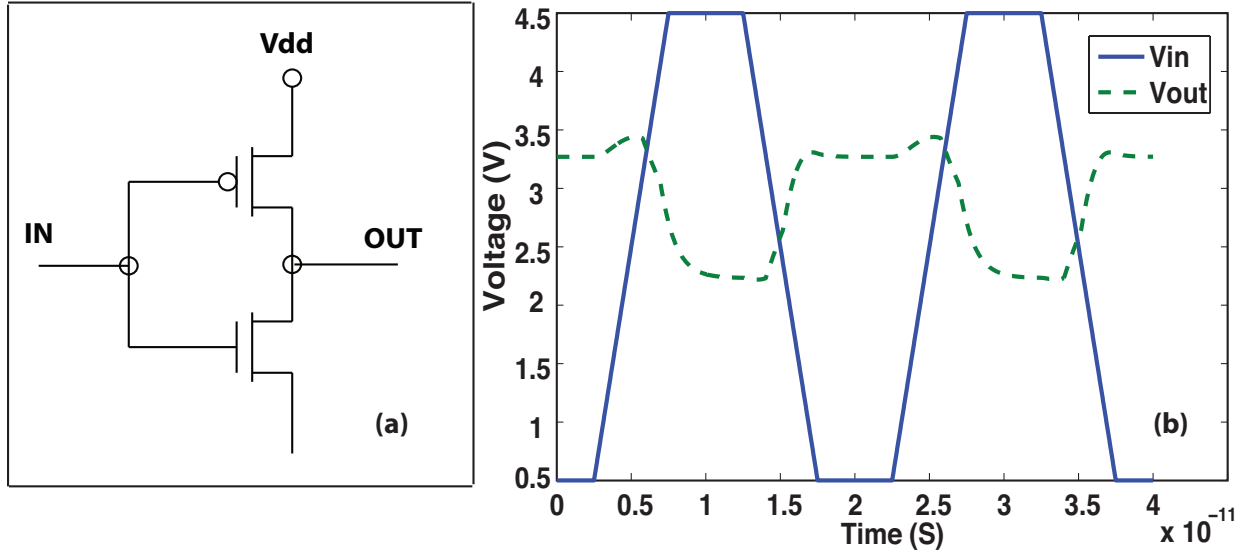


FIG. 6. (a) Circuit diagram of inverter. (b) Simulated I/O voltages with the generated compact model.

IV. MULTI-SCALE EDA SCHEME

Given the creative feature of the research field and the far greater quantum complexity of the nanoscale systems, it becomes very important for computational scientists to work closely with the engineers on developing the next generation multi-scale EDA technology which is proficient in both the nano-scale insights and the application scale. In addition, experiments have become increasingly difficult and expensive, and thus may not be a viable solution in the long term. Recognizing these facts, we devise a multi-scale simulation-based EDA flow as illustrated in Fig. 7. The flow starts from the most fundamental ab-initio characterization of nano-scale structures, goes all the way up to the classical modeling of semiconductor devices and compact modeling generation for large-scale SPICE simulation. The QM/EM scheme bridges the two regimes which have long been isolated. The success of this flow enables the first-principles accuracy to come into the chip-level simulation and the engineers' world. In the longer term, the seamless connection between the atomistic first-principles quantum mechanical calculation and the circuit simulation that is bridged by the QM/EM method can be further enhanced by the rapid development of computational power.

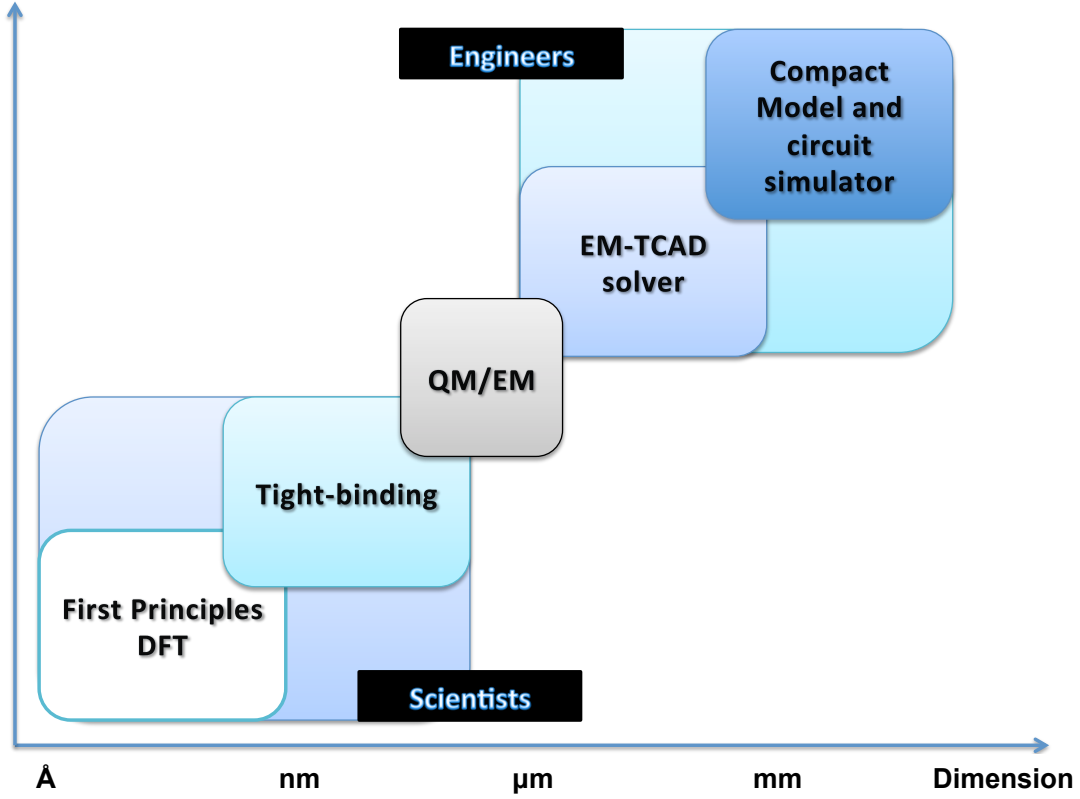


FIG. 7. Hierarchy of the multi-scale EDA flow.

V. CONCLUSION

We have presented the development of a new generation of simulation tools with the aim of providing the atomistic level of understanding capability for circuit design and with the hope that these tools may help us to design new devices and circuits. The aim is to package these tools in such a way that any experimentalists, device and circuit design engineers will be able to access the technology without requiring any specialist. Application to the simulation of junctionless transistor has demonstrated in principle the viability of the new EDA flow. The EDA tool starting from atomistic quantum mechanical simulation all the way to integrated circuit design of sub-16nm may thus be possible. Designing electronic devices on computer screen may not be a distant reality.

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